Amendments to the Claims

Claim 1. (original) A microprocessor for executing instructions obtained from an instruction store, said microprocessor comprising:

a) means for fetching instruction sets from an instruction store, each instruction set including an instruction;

b) means, coupled to said fetching means, for buffering instruction sets, said buffering means including a first buffer and a second buffer; and

c) means, coupled to said first and second buffers, for executing instructions, said executing means including register file means for storing data in a plurality of registers, a plurality of functional unit means for processing data wherein each said functional unit means processes data in a predetermined manner, bus means for providing plural data routing paths between said register file means and said plurality of functional unit means, and means for controlling the execution of instructions.

Please cancel claims 2-7.

This listing of claims will replace all prior versions, and listings of claims in the application.